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Title: **Implementation for a High Speed PHY for the 2.4 GHz band**

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Author: Bob Rood
Harris Semiconductor
2401 Palm Bay Road
Palm Bay, Florida
32905
USA
Tel: (407)-724-7000
Fax: (407)-724-7886
email: rrood@harris.com

This paper will detail the RF and analog design of the PRISM™ 11Mbps PC Card Wireless LAN card. Figure 1 shows a block diagram of the 11Mbps radio design. This Direct Sequence Spread Spectrum (DSSS) radio has been designed to provide data rates of 1, 2, 5.5, and 11Mbps. The 5.5 and 11Mbps waveforms are interoperable with the existing IEEE 802.11 specification for DS 1 and 2Mbps data rates and FCC rules that cover the operation at 2.4GHz for DSSS modulation.

PRISM™ Reference Radio High Rate

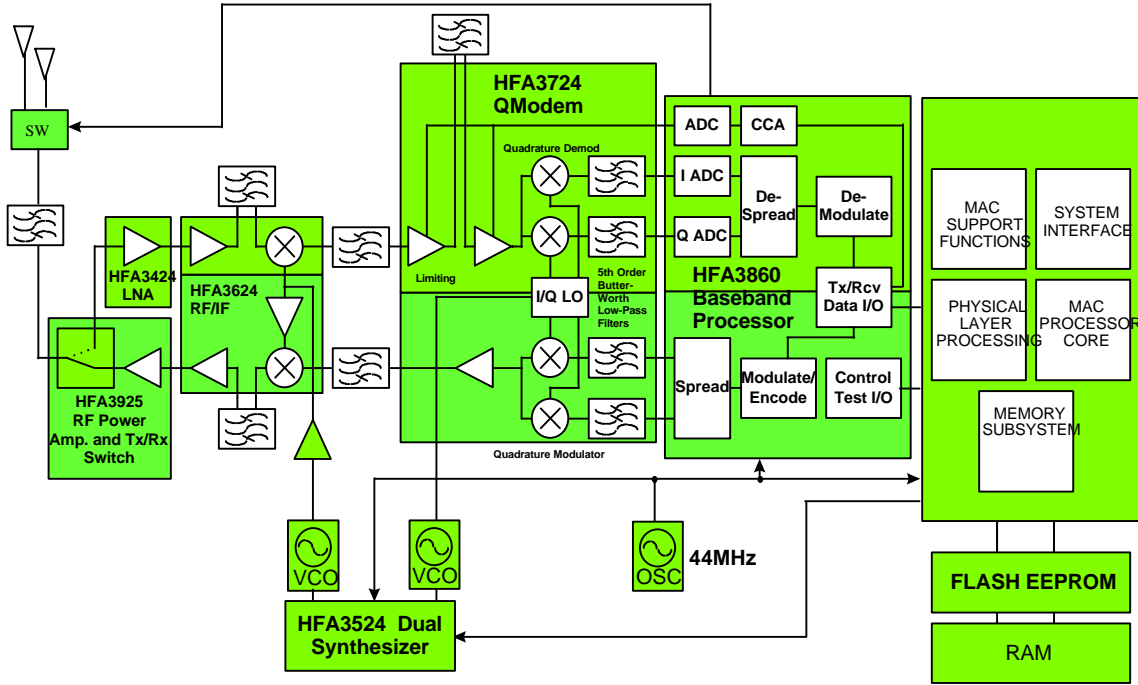


FIGURE 1. PRISM™ 11Mbps PC Card Block Diagram

The specifications of the PC Card Wireless LAN are as follows:

General Specifications

Targeted Standard	IEEE 802.11 Interoperable
Data Rate	1 Mbps DBPSK 2 Mbps DQPSK 5.5Mbps BMBOK 11Mbps QMBOK
Frequency Range	2412MHz to 2484MHz
Step Size	1MHz
IF Frequency	280MHz

IF Bandwidth	17MHz
RX/TX Switching Speed	2us (Typ)
Operating Voltage	4.5VDC - 5.5VDC
Operating Current	290mA (w/o pwr saving)(Note 1) 60mA (w pwr saving)(Note 2)
Standby Current	190mA at 1us Recovery (Note 3) 70mA at 550us Recovery (Note 3) 60mA at 2ms Recovery (Note 3) 30mA at 5ms Recovery (Note 3)
Operating Temperature Range	0oC to 70oC
Storage Temperature Range	-55oC to 125oC
Mechanical	Type II PCMCIA Card with Antenna Extension
Antenna Interface	SMA, 50 ohm

Receive Specifications

Sensitivity	-93dBm (Typ), 1 Mbps, 8E-2 FER (Note 4) -90dBm (Typ), 2 Mbps, 8E-2 FER (Note 4) -87dBm (Typ), 5.5Mbps, 8E-2 FER (Note 4) -84dBm (Typ), 11Mbps, 8E-2 FER (Note 4)
Input Third Order Intercept Point	-17dBm (Typ)
Image Rejection	80dB (Typ)
IF Rejection	80dB (Typ)
Adjacent Channel Rejection	35dB (Min) at 25MHz Offset
Supply Current	287mA (Typ), 11Mbps

Transmit Specifications

Output Power	+18dBm (Typ)
Transmit Spectral Mask	-32dBc (Typ) at First Side-Lobe
Supply Current	488mA (Typ), 11Mbps , 100% Duty Cycle

Notes:

1. 2% transmit, 98% receive without power savings mode.
2. 2% transmit, 8% receive, 90% standby with power savings mode
3. Recovery times do not include MAC recovery. Refer to Application Note "PRISM™ Power Management Modes" AN9665.
4. FER = Frame Error Rate or Packet Error Rate

Receive Processing

Referring to the block diagram in Figure 1, the schematic in Appendix A, and the bill of materials in Appendix B, a single antenna is used. Up to two antennas are supported in the HFA3860 [1] Baseband Processor to implement diversity, countering the adverse effects of multi-path fading. As space is at a premium in a PCMCIA Card environment, only one antenna is used. In an actual system implementation, if one can achieve diversity in at least one end of a link, such as at the access point where it is possible to achieve physical separation between diversity antennas, multipath performance will be improved.

From the antenna, the received input is applied to FL1, a Toko TDF2A-2450T-10 two pole dielectric bandpass filter, which is used to provide image rejection for the receiver. The IF frequency is 280MHz, and low-side injection is used, thereby placing the received image 560MHz below the tuned channel. FL1 also provides protection for the RF front-end from out of band interfering signals.

The T/R switch is integrated in the HFA3925 [2] RF Power Amplifier (RPA). The HFA3925 RPA operates from the unregulated 5V PC Card supply.

Following the T/R switch, the HFA3424 [3] Low Noise Amplifier (LNA) is used to set the receiver noise figure. The HFA3424 LNA operates from a regulated 3.5V supply. A logic-level PMOS switch, RF1K49093 [7], is used to control the drain supply voltage to the HFA3424 LNA, and implement a power down mode when transmitting.

A trade-off between noise figure and input intercept point exists in any receiver, to balance these conflicting requirements in the PRISM™ radio, an attenuator follows the HFA3424 LNA. The attenuation chosen is 5dB. To improve noise figure, this attenuation may be reduced; alternatively, to improve input intercept point, this attenuation may be increased. The cascaded front-end noise figure, input intercept point, and gain distribution analysis is shown in Table 1.

Next, the signal enters the HFA3624 [4] RF/IF Converter LNA section, which aids in setting receiver NF. FL2 is used to suppress image noise generated in both the HFA3424 LNA and the HFA3624 LNA, and is a Murata LFJ30-03B2442B084 two pole monolithic LC bandpass filter. Only modest attenuation at the image frequency is required. The insertion loss is not critical, since at this point in the receiver, component loss or NF is offset by the preceding gain stages. All sections of the HFA3624 RF/IF Converter operate from a regulated 3.5V supply.

Down-conversion from the 2.4GHz - 2.5GHz band is performed in the HFA3624 RF/IF Converter mixer section. As previously mentioned, the IF center frequency is 280MHz, and low-side local oscillator (LO) injection is used. A discrete LC matching network is used at the mixer output to differentially combine the IF outputs, as well as impedance match to a 50 ohm environment. A trimmer capacitor is used as part of the narrow-band matching network. An alternative, broadband matching network is described in the HFA3624 RF/IF Converter Application Note [5], and does not require any tunable elements. A direct impedance match to the IF filter, FL3 could be implemented if desired. The 50 ohm environment was chosen to allow ease in measurement of portions of the radio with external test equipment. An analysis of the mixer spurious responses is shown in Appendix C. There are no crossing spurious responses, therefore only tuned responses are shown.

The IF receive filter, FL3, is a Toyocom TQS-432 SAW bandpass filter. The center frequency is 280MHz, the 3dB bandwidth is 17MHz, and the differential group delay is less than 100ns. Insertion loss is typically 6dB, making it ideal for single-conversion systems. The impedance of the SAW is 270 ohm, and a series 33nH inductor is used to match the filter input to 50 ohm. The SAW output is matched directly to the IF input of the HFA3726 [6] Quadrature IF Modulator/Demodulator, using a shunt 56nH inductor. This presents a 250 ohm source impedance to the limiter input, thereby optimizing the limiter's NF. Measured performance of the SAW filter is shown in Appendix D.

In the receive mode, the HFA3726 Quadrature IF Modulator/ Demodulator provides two limiting amplifiers, a quadrature baseband demodulator, and two baseband low pass filters. All sections of the HFA3726 operate from a regulated 3.5V supply. The first limiting amplifier establishes the NF of the IF strip at approximately 7dB. A discrete one pole LC differential filter, FL4, is placed between the two limiters to restrict the noise bandwidth of the first limiter. As both limiters exhibit a broadband response,

with over 400MHz bandwidth, a noise bandwidth reduction filter is appropriate to ensure that the second limiter is fully limiting on the front-end noise within the signal bandwidth, as opposed to the broadband noise generated by the first limiter. This filter has a center frequency of 280MHz, and a 3dB bandwidth of 50MHz. It consists of a fixed 10nH inductor and a fixed 20pF capacitor, as described in the HFA3726 data sheet.

An additional limiter filter FL4A was added for the 11M bit data rate application at the output of the second limiter. This filter is needed to shape the hard limited, clipped, limiter 2 output into a more sinusoidal waveshape to restore phase and amplitude balance of the data vectors. This filter is a low pass with gain peaking at 280MHz.

The gain distribution/limiter noise analysis is shown in Appendix G. If the alternative HFA3624 broadband matching network is used, the HFA3624 mixer conversion gain will be higher, which will help ensure that the second limiter is fully limited on front-end noise.

At the output of the limiters, a $200\text{mV}_{\text{p,p}}$ differential signal level is maintained under all input conditions. This limited signal is then mixed in quadrature to baseband in the HFA3726 Quadrature IF Modulator/Demodulator. The LO needed for the quadrature mixing is applied at twice the IF frequency, or 560MHz. A divide by two circuit then provides an accurate quadrature LO for the mixers. The baseband outputs of the quadrature mixers are AC coupled off-chip to the integrated fifth order Butterworth filters. The output levels of the low pass filters are nominally $500\text{mV}_{\text{p,p}}$ single-ended, and are intended to be AC coupled to the HFA3860 Baseband Processor. The AC coupling time constant for 11Mbps QMBOK must be longer than that required for 2Mbps QPSK modulation due to more low frequency content and is implemented with 0.22uF series capacitors. These coupling capacitors must be taken into account, however, when estimating the time it takes to power up or awaken from sleep mode.

At the input to the HFA3860 Baseband Processor, the quadrature signals are analog to digital converted in wideband 3 bit converters. The sample rate is 44MSPS, which results in four samples per chip. A 44MHz Fox F4106 crystal oscillator is used to provide the main clock for the HFA3860. The signals are spread spectrum with no DC term, so it is feasible to AC couple the signals to the ADCs and avoid DC bias offsets. The signal at this point has been limited to a constant IF amplitude and then passed through two separate mixer and low pass filter paths. The component variations in these two paths can introduce offsets in amplitude and phase and can also use up some of the headroom in the ADCs. The maximum amplitude variation is 2dB and the maximum phase balance variation is 4 degrees. Since the signal is limited, the IF signals will have low peak to average ratios even with noise as an input. The I and Q signals will have sinusoidal properties with PSK modulation imposed. It is their combined vector magnitude that is limited, not their individual amplitudes. To optimize the demodulator's performance, the ADCs are operated at the point where they are at full scale on either I or Q one third of the time. To maintain this operating point in the face of component variations, there is an optional active adjustment of the ADC reference voltage by feedback. This avoids the necessity of allowing extra headroom for the variation. The adjustment circuit is very slow and averages the energy from the two channels over both packet and noise conditions.

The HFA3860 Baseband Processor correlates the PN spread symbols, then demodulates the DBPSK, DQPSK, BMBOK, or QMBOK symbols. The demodulator includes a frequency tracking loop that tracks and removes the carrier frequency offset. In addition it tracks the symbol timing, and differentially decodes (where appropriate) and descrambles the data. The data is output through the RX Port to the external processor.

The PRISM™ baseband processor, HFA3860 uses differential demodulation for the initial acquisition portion of the DBPSK header and then switches to coherent demodulation for the rest of the acquisition and data demodulation. The part then uses time invariant correlation to strip the PN spreading and phase processing to demodulate the resulting signals in the header and DBPSK/DQPSK demodulation modes.

In the 1Mbps DBPSK mode, data demodulation is performed the same as in header processing. In the 2Mbps DQPSK mode the demodulator demodulates two bits per symbol and differentially decodes these bit pairs. The bits are then serialized and descrambled prior to being sent to the output.

In the MBOK modes, the receiver uses a complex multiplier to remove carrier frequency offsets and a bank of serial correlators to detect the modulation. A biggest picker finds the largest correlator in the I and Q channels and determines the sign of those correlations. For this to happen, the demodulator must know absolute phase which is determined by referencing the data to the last bit of the header. Each symbol demodulated determines 1 or 2 nibbles of data. This is then serialized and descrambled before passing to the output.

In 1Mbps and 2Mbps modes the radio uses a spread spectrum signal with 10.4dB of processing gain ($10 \log(11 \text{ chip PN})$), the signal to noise ratio (SNR) in the chip rate bandwidth is approximately 0dB when the demodulator is at $1E-5$ bit error rate (BER) in BPSK. The radio operates with about 2.5dB of implementation loss relative to theoretical performance and achieves a sensitivity of -93dBm in the BPSK mode of operation.

Since the 11Mbps QMBOK modulation carries 11 times as many bits as the 1Mbps DBPSK case, in the same bandwidth, the energy per bit is 11 times less. Therefore the 11Mbps mode requires 10.4dB ($10 \log(11 \text{ Mb}/1 \text{ Mb})$) greater SNR (defined as ES/N_0) for the same bit error rate. In addition, QMBOK modulation is slightly more efficient than DBPSK by approximately 1.6dB. This gives a SNR increase for 11Mbps QMBOK modulation of 8.8dB when the demodulator is at $1E-5$ BER. This results in a typical sensitivity of -84dBm in the 11Mbps QMBOK mode and -87dBm for 5.5Mbps BMBOK mode.

The HFA3860 Baseband Processor provides decoding and descrambling of the data to prepare it for the Media Access Controller (MAC). All packet signals have a preamble followed by a header containing a start frame delimiter (SFD), other signal related data and a cyclic redundancy check (CRC). The MAC processes the header data to locate the SFD, determine the mode and length of the incoming message and to check the CRC. The MAC then processes the packet data and sends it on through the PC Card interface to the host computer. The MAC checks the packet data CRC to determine the data purity. If corrupted data is received, a retransmission is requested by the MAC which handles the physical layer link protocols.

Transmit Processing

Data from the host computer is sent to the MAC via the PC Card interface. Prior to any communications, however, the MAC sends a Request to Send (RTS) packet to the other end of the link and receives a Clear to Send (CTS) packet. The MAC then formats the payload data packet (MPDU) by appending it to a preamble and header and sends it on to the HFA3860 Baseband Processor which clocks it in. The HFA3860 Baseband Processor scrambles the packet and applies the selected spread spectrum modulation.

The modulator can support data rates of 1, 2, 5.5 and 11Mbps. The data can be either DPSK modulated at 1 MSPS (Million Symbols Per Second) or MBOK modulated at 1.375 MSPS and utilizes a baseband quadrature signal with I and Q components for all modulation modes. The DPSK spreading uses an 11 chip Barker sequence that is clocked at 11MHz. While the MBOK modulation takes the scrambled data and partitions it into nibbles (4 bits). For Binary MBOK modulation (5.5Mbps) one nibble is used per symbol and for Quaternary MBOK (11Mbps) two are used. The data is not differentially encoded, just scrambled, in these modes.

These are then output to the HFA3726 as CMOS logic signals. Following the RTS/CTS/MPDU is an acknowledge (ACK) packet by the receiving side of the link.

Transmit quadrature single-bit digital inputs are applied to the HFA3726 Quadrature IF Modulator/Demodulator from the HFA3860 Baseband Processor. These inputs are internally attenuated and DC coupled to the fifth order Butterworth low pass filters, which are used to provide shaping of the phase shift keyed (PSK) signal. The required transmit spectral mask, at the antenna, is -30dBc at the first side-lobe relative to the main-lobe. An unfiltered PSK waveform would have the first side-lobe suppressed only -13dBc. The fifth-order filters are tuned to an approximate 7.7MHz cutoff, using a 909 ohm fixed tuning resistor external to the HFA3726.

In the PC Card wireless LAN, the goal is to control the regrowth of the side-lobes, with the HFA3925 RFPA dominating the regrowth. This will result in maximum transmitted power available. To achieve this goal, once the PSK waveform is filtered at baseband, all remaining transmit elements are operated at a 6dB back-off from compression, except for the HFA3925 RFPA, which is operated at less back-off.

The low pass filters provide initial shaping of the PSK waveform. Final shaping is provided by a transmit IF filter, FL5, a Toyocom TQS-432 SAW bandpass filter. The low pass filter outputs are off-chip AC coupled to the quadrature up-converter in the HFA3726. The baseband AC coupling is implemented with 0.1uF series capacitors. The same twice IF frequency LO used previously is also used in this up-conversion. The IF output of the HFA3726 is reactively matched to FL5, with a 250 ohm resistive load presented to the HFA3726. A shunt 27nH inductor, in parallel with a 316 ohm resistor, is used to provide this match, to negate the effects of board and component capacitance, and provide a DC return to VCC to prevent saturation in the IF output stage of the HFA3726.

The output of FL5 is terminated in a 200 ohm potentiometer that is used for transmit gain control. A shunt 39nH inductor is used to negate the effects of parasitic board and component shunt capacitance, as well as match the SAW output to the potentiometer. This potentiometer has its center wiper connected to the HFA3624 RF/IF Converter transmit IF input, which has an input resistance of approximately 3k ohm. By varying the potentiometer, the gain of the transmit chain is controlled, allowing for precise control of the signal back-off at the HFA3925 RFPA. Therefore, this potentiometer is adjusted to achieve the desired compromise between transmit output power and the main lobe to side lobe ratio of the output PSK waveform, typically -32dBc to -35dBc, at an output power of +18dBm.

Up conversion to the 2.4GHz - 2.5GHz band is performed in the HFA3624 RF/IF Converter transmit mixer. The mixer output is filtered with FL6, a Murata LFJ30-03B2442B084 two pole monolithic LC bandpass filter. This filter suppresses the LO feedthrough from the mixer, and selects the upper sideband. The transmit buffer in the HFA3624 RF/IF Converter amplifies the selected sideband, easing the requirement for HFA3925 RFPA gain.

FL7, a Toko TDF2A-2450T-10 two pole dielectric bandpass filter, is used to further suppress both the transmit LO leakage and the undesired sideband.

The HFA3925 RFPA amplifies the transmit signal to a level of approximately +20dBm, as measured at the T/R switch output. This represents a back-off from 1dB compression of approximately 4.5dB.

Transmit side-lobe performance is approximately -32dBc to -35dBc with this level of back-off. Allowing for approximately 2dB of loss between the T/R switch output and the antenna connector results in a final output power of +18dBm.

The HFA3925 RFPA is the only physical layer component that operates directly from the 5V PC Card supply. To supply the needed negative gate bias to the HFA3925 RFPA, a ICL7660SIBA [7] charge pump is used. A second potentiometer is used to adjust the drain current on the third stage of the HFA3925 to a quiescent operating current of 90mA, as measured through a one ohm sense resistor. A base-emitter junction is used as part of the gate bias network to provide temperature compensation, and all three gates are driven from one source to reduce the impact of process variation on pinch-off voltage. The nominal quiescent drain bias currents are 20mA for stage one, 53mA for stage two, and 90mA for stage three.

A second logic-level PMOS switch, RF1K49093, is used to control the drain supply voltage to the HFA3925 RFPA, and implement a power down mode when receiving. A 2N2222 NPN transistor is used to level shift the 3.5V logic level from the MAC to drive the 5V PMOS switch gates, as well as the 5V HFA3925 RFPA T/R control gate. The T/R Vdd pin is connected to the three PA Vdd pins, and is powered down in the receive mode by the PMOS switch. In this manner the T/R control pin transfer characteristic is less dependent on it's voltage, with the receive state being valid for T/R control voltages as low as 3 volts. If the T/R VDD pin was connected to a supply in both transmit and receive modes, the T/R control voltage would have to be within a few hundred millivolts of the supply to obtain similar performance.

Following the T/R switch, FL1 is reused in the transmit mode to attenuate harmonics generated in the HFA3925 RFPA, as well as providing additional suppression of the LO. As the loss of FL1 is approximately 2dB, the amount of transmit power available at the antenna is approximately +18dBm.

As the transmit chain is operated linearly, any gain flatness from the HFA3624 and HFA3925, as well as from FL6, FL7, and FL1, will result in the transmit output power varying across the operating channels. To reduce the amount of variability, three 1pF capacitors are used as coupling elements to provide a form of simple equalization. Care must be exercised to ensure that the filter rejection is still acceptable in meeting the requirements of FCC 15.247. If desired, more complicated equalization could be used to maintain an improved 50 ohm environment for all passband frequencies. Using the simple equalization, the transmit output varies approximately 2.5dB across the band.

Synthesizer Section

The dual frequency synthesizer section uses the HFA3524 [9] Synthesizer and two voltage controlled oscillators to provide a tunable 2132MHz to 2204MHz first LO, and a fixed 560MHz second LO. Both feedback loops use a 1MHz reference frequency that is derived from the 44MHz Fox F4106 crystal oscillator. Isolation of the HFA3524 synthesizer 44MHz clock from the HFA3860 clock line is accomplished with a 560 ohm resistor and careful layout. Both feedback loops are fourth order (four poles in the transfer function) and were designed to have loop bandwidths of 10kHz, and phase margins of 50 degrees. The feedback loop analysis is included for both loops in Appendix E. Measured phase noise performance and calculated RMS phase jitter is included in Appendix F. All components in the synthesizer section operate from a regulated 3.5V supply.

The tunable 2132MHz to 2204MHz first LO oscillator is a Motorola KXN1332A VCO. To ensure operation at low tuning voltages, a start-up circuit was added to force the tuning voltage from the HFA3524 Synthesizer RF charge pump to a high state for a short period (~1ms) following HFA3524 programming. A 2N2907 PNP transistor was used to implement this function, and the MAC device provides the control signal. The output level of the first LO to the HFA3624 RF/IF Converter is attenuated to approximately -3dBm. An active buffer using an additional HFA3424 is used to provide additional isolation between the VCO and the HFA3624 LO input.

The fixed 560MHz second LO oscillator is a discrete design, using a Phillips BFR505 transistor and a Siemens BBY51 varactor, as described in the HFA3524 Synthesizer evaluation board documentation. The output level of the second LO to the HFA3724 Quadrature IF Modulator/Demodulator is attenuated to approximately -6dBm and a three pole low pass filter is included to preserve the duty cycle of the output. High even order components in the second LO can result in offsets from a 50% duty cycle, and will

degrade the quadrature phase accuracy of the HFA3726. A transconductance network is used at the HFA3726 LO input to convert the second LO voltage into a current, as recommended in the HFA3726 data sheet. As the HFA3524 Synthesizer auxiliary IF input covers the 560MHz range, the internal divide-by-two LO buffer output of the HFA3726 is disabled, as recommended in the HFA3726 data sheet.

Regulator Section

Linear voltage regulators are used to provide filtering and isolation from the 5V PC Card input supply. An additional advantage of using voltage regulators is a savings in overall supply current, as all of the components that are regulated consume less current at a 3.5V operating point, as opposed to a 5V operating point. The 3.5V operating point was chosen specifically as the lowest voltage that would support the MAC controller.

The only components operating directly from the 5V supply are the HFA3925 RFPA, in order to maximize RF output power, and the PCMCIA Card interface sections of the MAC controller.

A total of three regulators, 3.5V Toko TK11235MTL, are used in the PC Card wireless LAN. One regulator supplies voltage to the HFA3860 Baseband Processor and portions of the MAC, as well as the HFA3424 LNA and HFA3624 RF/IF Converter. A second regulator supplies voltage to the synthesizer. The third regulator supplies voltage to the HFA3726 Quadrature IF Modulator/Demodulator.

PCB Layout Guidelines

Although the actual PCB layout is proprietary, some of the techniques utilized are worthy of discussion [10]. As there are many RF, IF, analog, and digital circuits in close proximity, isolation is of prime concern. All RF and IF circuits utilize coplanar waveguide with ground transmission line techniques to allow for easy integration of varied line widths and component pin widths, and to provide a low dispersion, high isolation environment. A Radio Schematic is available on the Internet at <http://www.semi.harris.com/prism/lanref.htm>.

The outside two planes of each side of the PCB are dedicated to RF and IF signal processing, and form two pairs of coplanar waveguide with ground circuits. As the two sides of the PCB contain circuitry that must be isolated from each other, blind via techniques are used, and the only places that the two sides share common ground or signal connections are when signals are passed between them, mainly when LO1 and LO2 need to pass from the synthesizer side to the RF/IF transceiver side.

In general, the RF and IF circuit layouts need to be as short and direct as possible to avoid costly shielding. This is especially critical in the receive IF stages where spurious signal coupling can easily occur, resulting in poor sensitivity or high packet error rates.